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TITLE

PROCESS FOR INTEGRATING ALIGNMENT MARK AND TRENCH DEVICE

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates in general to a semiconductor process. More particularly, it relates to a simplified process for integrating an alignment mark and a trench device to reduce fabrication cost.

Description of the Related Art:

Lithography is one of most important processes for fabricating semiconductor integrated circuits. Lithography is used in the transfer of a pattern onto a thin film or the fabrication of a mask for ion implantation. In general, lithography is conducted many times in the production of semiconductor circuits. In a lithography step, however, one critical factor is pattern alignment. When a wafer is processed to form patterns in the different thin films deposited thereon, the wafer must be properly aligned relative to the previous pattern. Conventionally, an alignment mark (AM) is used for alignment before carrying out photo-exposure.

In general, alignment marks are formed outside the device region, such as the scribe line of a wafer, at the same time as a thin film such as an insulating layer or a conductive layer is patterned. FIGS. 1a to 1d are cross-sections showing a conventional process for integrating an alignment mark and a trench device. First, in FIG. 1a, a

substrate 100, such as a silicon wafer, is provided. The substrate 100 has a device region 10 and an alignment mark region 20 which is at the scribe line of the wafer 100.

Next, a patterned masking layer 105 is formed on the substrate 100. The patterned masking layer 105 can be composed of a pad oxide layer 102 and a thicker overlying silicon nitride layer 104. Next, the substrate 100 is etched using the patterned masking layer 105 as an etch mask to form deep trenches 110a and 110b therein. The deep trench 110a is on the device region 10 and the trench 110b having a width larger than the deep trench 110a is on the alignment mark region 20.

Next, trench capacitors 118a and 118b are respectively formed in the lower portion of the deep trenches 110a and 110b. The trench capacitor 118a includes a top plate 116a, a capacitor dielectric layer 114a, and a bottom plate 112a. Also, the trench capacitor 118b includes a top plate 116b, a capacitor dielectric layer 114b, and a bottom plate 112b. Next, collar insulating layers 117a and 117b are respectively formed on the trench capacitors 118a and 118b and over the sidewall of the deep trenches 110a and 110b. Thereafter, conductive layers 120a and 120b, such as polysilicon, are respectively formed in the deep trenches 110a and 110b, which have a height substantially equal to the collar insulating layers 117a and 117b.

Next, a conductive layer 122, such as polysilicon, is formed on the masking layer 105 and fills in the deep trenches 110a and 110b.

Next, in FIG. 1b, chemical mechanical polishing (CMP) is performed on the conductive layer 122 to respectively

leave a portion of the conductive layers 122a and 122b in the deep trenches 110a and 110b.

Next, in FIG. 1c, the conductive layers 122a and 122b are etched to leave a portion of the conductive layers 124a and 124b in the deep trenches 110a and 110b, respectively. The conductive layer 120a and the remaining conductive layer 124a in the deep trench 110a are used as a wiring layer for the trench capacitor 118a. In addition, the trench capacitor 118b, the conductive layer 120b, and the remaining conductive layer 124b are used as an alignment mark.

Since the trench capacitor 118b and the conductive layers 120b and 124b are formed in the deep trench 110b, the step height of the substrate 100 on the alignment mark region 20 is reduced, lowering the image contrast of the alignment mark.

Accordingly, in FIG. 1d, a patterned photoresist layer (not shown) is formed on the masking layer 105 by lithography to completely cover the deep trench 110a and expose the deep trench 110b only. Thereafter, the conductive layer 124b is completely removed and then the underlying conductive layer 120b and the collar insulating layer 117b are partially removed by etching using the patterned photoreist layer as a mask to leave a portion of the conductive layer 120c and the collar insulating layer 117c, thereby increasing the step height of the substrate 100 on the alignment mark region 20. However, such a process is complex, thus increasing fabrication cost and the time required thereby.

SUMMARY OF THE INVENTION

Accordingly, an object of the present invention is to provide a novel process for integrating an alignment mark and a trench device, thereby simplifying the process to reduce fabrication cost and time and increase throughput.

According to the object of the invention, a process for integrating an alignment mark and a trench device are provided. First, a substrate having first and second trenches is provided, wherein the second trench used as the alignment mark is wider than the first trench. Next, the trench device is formed in each of the low portions of the first and second trenches, and then a first conductive layer is formed on the trench device in each of the first and second trenches. Thereafter, a second conductive layer is formed overlying the substrate filling in the first trench and is simultaneously and conformably formed over the inner surface of the second trench. Finally, the second conductive layer and a portion of the first conductive layer in the second trench are removed and simultaneously leave a portion of the second conductive layer in the first trench by an etch back process, wherein the etch back process employs chemical mechanic polishing to remove the second conductive layer overlying the substrate.

Moreover, the first and second conductive layers can be a polysilicon layer, which have a thickness of about 2000Å to 4000Å.

DESCRIPTION OF THE DRAWINGS

The present invention will become more fully understood from the detailed description given hereinbelow and the accompanying drawings, given by way of illustration only and thus not intended to be limitative of the present invention.

FIGS. 1a to 1d are cross-sections showing a conventional process for integrating an alignment mark and a trench device.

FIGS. 2a to 2f are cross-sections showing a process for integrating an alignment mark and a trench device according to the invention.

DETAILED DESCRIPTION OF THE INVENTION

A preferred embodiment of the present invention is now described with reference to FIGS. 2a to 2f. First, in FIG. 2a, a substrate 200, such as a silicon wafer, is provided. The substrate 200 has a device region 30 and an alignment mark region 40 which is at the scribe line of the wafer 200.

Next, a masking layer 205 is formed on the substrate 200. As shown in FIG. 2a, the masking layer 205 can be composed of a pad oxide layer 202 and a thicker overlying silicon nitride layer 204. In this invention, the pad oxide layer 202 has a thickness of about 100Å and can be formed by thermal oxidation or conventional CVD, such as atmospheric pressure CVD (APCVD) or low pressure CVD (LPCVD). Moreover, the silicon nitride layer 204 overlying the pad oxide layer 202 has a thickness of about 1000~2000Å and can be formed by LPCVD using $SiCl_2H_2$ and NH_3 as reaction sources.

Next, a photoresist layer 206 is coated on the masking layer 205, and then the photoresist layer 206 is patterned by lithography to form openings 208a and 208b therein. The opening 208a is in the device region 30 and the opening 208b having a width larger than the opening 208a is in the alignment mark region 40. Next, the masking layer 205 is anisotropically etched by, for example, reactive ion etching (RIE), using the patterned photoresist layer 206 as an etch mask to transfer the opening patterns 208a and 208b into the masking layer 205 and thus expose a portion of the substrate 200.

Next, in FIG. 2b, the patterned photoresist layer 206 is removed by a suitable wet chemical etching or ashing technique. Anisotropic etching, for example, RIE, is subsequently performed using the masking layer 205 as an etch mask. The silicon substrate 200 under these openings is etched to form deep trenches 210a and 210b having a predetermined depth in the silicon substrate 200. Also, the deep trench 210a is in the device region 30 and the trench 210b having a width larger than the deep trench 210a is on the alignment mark region 40.

Next, in FIG. 2c, trench devices 218a and 218b are respectively formed in the lower portion of the deep trenches 210a and 210b. In the invention, the trench devices 218a and 218b can be a trench capacitor. The trench capacitor 218a includes a top plate 216a, a capacitor dielectric layer 214a, and a bottom plate 212a. Also, the trench capacitor 218b includes a top plate 216b, a capacitor dielectric layer 214b, and a bottom plate 212b. The bottom plates 212a and 212b are formed in the substrate 200 around

the lower portion of the trenches 210a and 210b, respectively. The top plates 216a and 216b which can be composed of polysilicon are disposed in the lower portion of the deep trenches 210a and 210b, respectively. The capacitor dielectric layer 214a and 214b are respectively disposed between the bottom plates 212a and 212b and the top plates 216a and 216b.

Next, collar insulating layers 217a and 217b, such as silicon oxides, are respectively formed on the trench capacitors 218a and 218b and over the sidewall of the trenches 210a and 210b. Thereafter, a conductive layer (not shown), such as polysilicon, is formed on the masking layer 205 and fills in the deep trenches 210a and 210b by conventional deposition, such as CVD. A portion of the conductive layers 220a and 220b is left in the deep trenches 210a and 210b, respectively, by an etch back process. The height of the remaining conductive layers 220a and 220b are substantially equal to the collar insulating layers 217a and 217b which have a height of about 2000Å to 4000Å.

FIGS. 2d to 2f are cross-sections showing the critical step of the invention. In FIG. 2d, a conductive layer 222, such as polysilicon layer, is formed on the masking layer 205 and fills in the deep trench 210a on the device region 30. At the same time, the conductive layer 222 is also conformably formed on the masking layer 205 and the inner surface of the deep trench 210b on the alignment mark region 40. Here, the conductive layer 222 has a thickness of about 2000Å to 4000Å.

Next, in FIG. 2e, chemical mechanical polishing (CMP) is performed on the conductive layer 222 using the masking

layer 205 as a stop layer to leave a portion of the conductive layer 222a and 222b in the deep trenches 210a and 210b, respectively.

Finally, in FIG. 2f, the remaining conductive layers 222a and 222b are etched by isotropic etching, such as wet chemical etching. In this etch back process, the remaining conductive layer 222b on the alignment mark region 40 is completely removed and a portion of the conductive layer 220b and the collar insulating layer 217b is then removed to leave a portion of the conductive layer 220c and the collar insulating layer 217c, thus completing fabrication of the alignment mark. Here, the conductive layer 220b is completely removed to increase the step height of the substrate 200 on the alignment mark region 40, thereby increasing image contrast for lithography. At the same time, in this etch back process, the remaining conductive layer 222a on the device region 30 is partially removed to leave a portion of the conductive layer 222c. The remaining conductive layer 222c and the conductive layer 220a serve as a wiring layer for the trench capacitor 218a.

In addition, it is noted that since the conductive layer 222 is conformably formed over the inner surface, but does not completely fill the deep trench 210b, isotropic etching can be performed without previous CMP to further simplify the fabrication process.

According to the invention, the conductive layer 222 on the alignment mark 40 can be completely removed by the isotropic etching. Compared with the prior art wherein etching is performed at least twice and lithography is performed at least once to completely remove the conductive

layer 222, fabrication cost and time can be reduced through the simplified process of the invention, thereby increasing throughput.

While the invention has been described by way of example and in terms of the preferred embodiments, it is to be understood that the invention is not limited to the disclosed embodiments. To the contrary, it is intended to cover various modifications and similar arrangements (as would be apparent to those skilled in the art). Therefore, the scope of the appended claims should be accorded the broadest interpretation so as to encompass all such modifications and similar arrangements.